AMENDMENTS TO THE CLAIMS

1. (Withdrawn) A complimentary metal oxide semiconductor (CMOS) image sensor comprising:

a semiconductor substrate incorporating therein a p-type epitaxial layer formed by epitaxially growing up an upper portion of the semiconductor substrate;

a pixel array formed in one predetermined location of a semiconductor substrate, having a plurality of transistors and active areas therein; and

a logic circuit formed in the other predetermined location of the semiconductor substrate having active areas and at least one transistor for processing a signal from the pixel array, wherein a gate insulate or each transistor in the pixel array is thicker than a gate insulator of the transistor in the logic circuit.

2. (Withdrawn) The CMOS image sensor as recited in claim 1, wherein the gate insulator of each transistor in the pixel array employs a double layer having a first and second gate insulators and the gate insulator of the transistor in the logic circuit employs a single layer.

3. (Withdrawn) The CMOS image sensor as recited in claim 2, wherein the first gate insulator has a thickness ranging from about 10Å to about 40Å and the second gate insulator has a thickness ranging from about 50Å to about 60Å.

4. (Withdrawn) The CMOS image sensor as recited in claim 1, wherein the first gate insulator is silicon oxide (SiO_2) formed by thermally oxidizing the p-type epitaxial layer.

5. (Currently Amended) A method for manufacturing a CMOS image sensor, the method comprising the steps of:

a) preparing a semiconductor substrate incorporating therein a p-type epitaxial layer therein, wherein the semiconductor substrate is divided into two parts of which one part is defined as a pixel array having a number of pixels, each pixel containing a drive transistor, a select transistor, a transfer transistor and a reset transistor and the other part is defined as a logic

circuit, the pixel array being isolated from the logic circuit by means of a field oxide region therebetween;

b) forming a first gate insulator layer on a top surface of the p-type epitaxial layer;

c) forming a mask on a top face of the first gate insulator layer in the pixel array;

d) removing the first gate insulator layer in the logic circuit by using the mask;

e) removing the mask in the pixel array;

f) forming ~~the~~ a second gate insulator layer on the top face of the first gate insulator layer in the pixel array and a top face of the p-type epitaxial layer in the logic circuit; and

g) forming a plurality of photodiodes and a plurality of the drive transistors, the select transistors, the transfer transistors and the reset transistors in the pixel array based on the first and the second gate insulator layers and at least one transistor in the logic circuit based on the second gate insulator layer..

6. (Currently Amended) The method as recited in claim 5, wherein the first gate insulator layer has a thickness ranging from about 10Å to about 40Å and the second gate insulator layer has a thickness ranging from about 50Å to about 60Å.

7. (Original) The method as recited in claim 5, where in the step d) is carried out be means of a wet-etching process.

8. (Original) The method as recited in claim 7, where in the step d) is carried out by using an hydrofluoric acid (HF).

9. (Original) The method as recited in claim 7, where in the step d) is carried out by using a buffered oxide etchant (BOE).

10. (Original) The method as recited in claim 5, where in the step e) is carried out by using an O_2 plasma.

11. (Original) The method as recited in claim 5, wherein the step e) is carried out by using a sulfuric acid (H_2SO_4).

12. (Original) The method as recited in claim 5, wherein the step e) is carried out by using a thinner.

13. (Currently Amended) The method as recited in claim 5, where in the first gate insulator layer is SiO_2 formed by thermally oxidizing the p-type epitaxial layer.